



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,012	10/31/2003	Eric Adler	21806-00070-US1	8254
30678	7590	06/01/2006	EXAMINER	
CONNOLLY BOVE LODGE & HUTZ LLP SUITE 800 1990 M STREET NW WASHINGTON, DC 20036-3425				POMPEY, RON EVERETT
		ART UNIT		PAPER NUMBER
		2812		

DATE MAILED: 06/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

H.A

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/697,012

Filing Date: October 31, 2003

Appellant(s): ADLER ET AL.

Myron Keith Wyche
For Appellant

EXAMINER'S ANSWER

MAILED

JUN 1 - 2006

GROUP 2800

This is in response to the appeal brief filed March 10, 2006 appealing from the Office action mailed August 16, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,241,210	Nakagawa et al.	8-1993
6,118,152	Yamaguchi et al.	9-2000

3,813,586 Conner 5-1974

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 20 - 27 rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa et al. (US 5,241,210).

Nakaqawa discloses the limitations of:

forming first (59a and 54a fig. 17) and second diffusion regions in a semiconductor substrate; forming a trench (53, fig. 16) structure around said first and second diffusion regions; and forming a contact on said trench structure and said substrate (63a, fig. 17) for controlling current through said diffusion regions; and

forming first (61a, fig.17) and second gates over said first and second diffusion regions with source (56a, and 58a, fig. 17) and drain regions formed in said diffusion on each side of said gate (col. 7, Ins. 25-56 and col. 9, Ins. 36-48). It is inherent, to one of

ordinary skill in the semiconductor device art, that when an applied potential, voltage or current, across a contact in a particular diffusion region; a field is applied at that region which will increase or decrease the resistance across that region (see Conner, column 4, lines 7-10, for reference.

3. Claims 20 –27 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al. (US 6,118,152).

Yamaguchi discloses the limitations of:

forming first and second diffusion regions (the fox regions 13a and 13b, fig. 1 define the diffusion regions) in a semiconductor substrate; forming a trench (5, fig. 1) structure around said first and second diffusion regions; and forming a contact on said trench structure (19a and 19b, fig. 1) and said substrate (18, fig. 1) for controlling current through said diffusion regions; and

forming first (15a, fig.1) and second (15b, fig.1) gates over said first and second diffusion regions with source (9, 12a and 12b, fig. 1) and drain regions formed in said diffusion on each side of said gate (col. 3, ln. 25 - col. 5, ln. 4). It is inherent, to one of ordinary skill in the semiconductor device art, that when an applied potential, voltage or current, across a contact in a particular diffusion region; a field is applied at that region which will increase or decrease the resistance across that region (see Conner, column 4, lines 7-10, for reference.

(10) Response to Argument

The Appellant argues that:

a. Nakagawa et al. nowhere discloses a device with both a "trench structure" with a trench terminal connection 21 and "substrate" with substrate terminal connection 22, as in the present invention; wherein "said trench structure and said substrate receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region," as recited in claims 20 and in similar language in claim 26. However, Nakagawa discloses a trench (53, fig. 17) with an electrode formed on it and a substrate (54a, fig. 17) with an electrode (63a, fig. 17), wherein a control voltage is applied, which will create an electric field, as stated in the rejection above. The Nakagawa reference does not explicitly state that an electric field is produced, but this is an inherent feature when applying a voltage potential across a substrate. The appellant does not argue the inherent statement given by the examiner in the rejection, therefore it is taken that the inherency is not questioned and the rejection is valid. Additionally the appellant argues that the silicon on insulator(SOI) substrate would interfere with the electric field and negatively affect the operation of the invention. The appellant makes this general statement without proof that the insulator will interfere with the electric field. Even if the insulator did interfere with the electric field, which the examiner is not saying it does, that does not mean that the field, produced when the control voltage is applied, will not be strong enough to control the current in the diffusion region.

b. Yamaguchi et al. nowhere discloses a device with both a "trench structure" with a trench terminal connection 21 and "substrate" with substrate

terminal connection 22, as in the present invention; wherein "said trench structure and said substrate receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region," as recited in claims 20 and in similar language in claim 26. However, Yamaguchi discloses a trench (5, fig. 1) with an electrode (19a,b, fig. 1) formed on it and a substrate (8, fig. 1) with an electrode (18, fig. 1), wherein a control voltage is applied, which will create an electric field, as stated in the rejection above. The Yamaguchi reference does not explicitly state that an electric field is produced, but this is an inherent feature when applying a voltage potential across a substrate. The appellant does not argue the inherent statement given by the examiner in the rejection, therefore it is taken that the inherency is not questioned and the rejection is valid. Additionally the appellant argues that the position of the trench structure 8 and the gate electrodes 15b/15c, in Yamaguchi, would interfere and negatively affect the operation of the present invention. However, first the trench is structure 5 not structure 8, therefore the trench is not positioned as stated in the appellants' arguments and secondly the position of the trenches is not claimed and therefore has no bearing on the patentability of the claimed invention.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Ron Pompey

Ron Pompey

May 25, 2006

Conferees:

Mike Lebentritt



Ricky Mack

